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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,970	06/25/2003	Tong Tee Tan	70010721-2	6461

57299 7590 10/22/2007

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
10/22/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/606,970	TAN, TONG TEE	
	Examiner	Art Unit	
	Cynthia Britt	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the appeal brief filed on 7/6/07, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

JACQUES LOUIS-JACQUES
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims are rejected under 35 U.S.C. 102(e) as being anticipated by Reberga U.S. Publication No. 2004/0128603.

As per claim 1, Reberga teaches the claimed bit error detection circuit comprising: a predictor circuit that uses a plurality of bits of a bit sequence to predict a next bit in the sequence; a comparator circuit that compares an actual next bit in the sequence with the predicted next bit to determine whether there is any error in the actual next bit; (Abstract, paragraphs [0005-0007], and paragraphs [0045-0047]) and a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit (paragraph [0018] and paragraph [0053]).

As per claim 2 Reberga teaches the correction circuit comprises a circuit element that replaces the actual next bit with the corrected actual next bit in the plurality of bits (paragraph [0018] and paragraph [0053]).

As per claim 3, Reberga teaches the bit sequence comprises a pseudo-random bit sequence and the predictor circuit predicts the next bit by comparing two of the bits of the sequence (paragraph [0038] and paragraph [0045] Note: it is common in the art to use an exclusive-OR circuit as a comparator).

As per claim 8, Reberga teaches the claimed bit error detection circuit comprising: a shift register that receives N bits of a pseudo-random bit sequence (PRBS); a first logic element that receives output signals from two stages of the shift register and provides a signal indicative of a predicted (N+1)-th bit; a second logic element that receives the signal indicative of the predicted (N+1)-th bit and a signal

indicative of an actual (N+1)-th bit and provides an output signal indicative of any error in the actual (N+1)-th bit; and a third logic element that receives the output signal and corrects the actual (N+1)-th bit according to the output signal as the (N+1)-th bit propagates through the shift register (paragraphs [0044-0053])

As per claim 9, Reberga teaches the third logic element receives the actual (N+1)-th bit from one of the shift register stages, corrects said bit according to the output signal, and inserts said bit as corrected into another one of the shift register stages in place of the actual (N+1)-th bit (paragraph [0053]).

As per claim 14, Reberga teaches the claimed method of detecting errors in a bit sequence comprising: predicting a next bit of a bit sequence according to a plurality of previous bits of the sequence; comparing the predicted next bit with an actual next bit; and if the comparison indicates a difference between the predicted next bit and the actual next bit, providing an error signal (Abstract, paragraphs [0005-0007], and paragraphs [0045-0047]) and correcting the actual next bit (paragraph [0018] and paragraph [0053]).

As per claim 15, Reberga teaches correcting the actual next bit comprises replacing the actual next bit with the corrected actual next bit in the bit sequence (paragraph [0053] and claim 13).

As per claim 16 Reberga teaches the bit sequence comprises a pseudo-random bit sequence (paragraph [0038]).

As per claim 18, Reberga teaches determining whether any bit errors are detected during a predefined interval (paragraphs [0055-0056]).

As per claim 19, Reberga teaches measuring a period of time to determine when the predefined interval has elapsed (paragraphs [0055-0056]).

As per claim 20, Reberga teaches counting a predefined number of bits as they propagate through a circuit element to determine when the predefined interval has elapsed (paragraphs [0055-0056]).

As per claim 21, Reberga teaches the claimed bit error detector comprising: an actual next bit input that receives a plurality of bits of a bit sequence (paragraph [0038]); a predictor coupled to the input and having a predicted next bit output (paragraph [0045]); a comparator coupled to the predicted next bit output and to the actual next bit input, the comparator having an error signal output (paragraphs [0046-0047]); and a corrector coupled to the error signal output and having a corrected actual next bit output (paragraph [0053]).

As per claim 22, Reberga teaches the predictor comprises a predictor circuit for receiving the plurality of bits, for determining a predicted next bit from at least some of the plurality of bits, and for providing the predicted next bit at the predicted next bit output (paragraph [0045]); the comparator comprises a comparator circuit for receiving the predicted next bit and the actual next bit, for comparing the predicted next bit and the actual next bit (paragraph [0046]), and for providing an error signal at the error signal output when a difference is detected between the predicted next bit and the actual next bit; and the corrector comprises a correction circuit for receiving the error signal, producing a corrected actual next bit, and providing the corrected actual next bit at the corrected actual next bit output (paragraphs [0052-0053]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reberga U.S. Publication No. 2004/0128603 in view of Rakib et al. U.S. Publication No. 2001/0001616.

As per claim 23 Reberga substantially teaches the claimed invention having a pseudo-random bit sequence generator for creating a pseudo-random bit sequence (paragraph [0038]); a pseudo-random bit sequence error detector, for detecting and correcting any error in an actual next bit of the pseudo-random bit sequence, wherein the pseudo-random bit sequence error detector comprises: a predictor circuit that uses a plurality of bits of the pseudo-random bit sequence to provide a predicted next bit of the pseudo-random bit sequence (paragraphs [0045-0047]); a comparator circuit that

compares the actual next bit in the pseudo-random bit sequence with the predicted next bit to determine whether there is an error in the actual next bit; and a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit (paragraphs [0052-0053]). Not disclosed by Reberga is that this device is within a communications system.

However, in an analogous art, Rakib et al. teaches a communications system (Abstract), comprising: a pseudo-random bit sequence generator for creating a pseudo-random bit sequence (paragraph [0370]); a transmitter in signal communication with the pseudo-random bit sequence generator; a communications channel in signal communication with the transmitter, the transmitter for transmitting the pseudo-random bit sequence over the communications channel (paragraph [0371]); and a pseudo-random bit sequence error detector, in signal communication with the communications channel (paragraph [0026]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the bit sequence error detection/correction system disclosed by Reberga with the transmission system of Rakib et al. This would have been obvious as suggested by Rakib et al. (paragraph [0273]) where any known error detection and correction could be used with this system. Rakib also teaches predicting and comparison of the next bit (paragraphs [0438-0439]).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites in part "...a trigger circuit that activates the correction circuit when the predictor circuit contains a plurality of bits in which no erroneous bits have been detected." It is unclear why a correction circuit would be activated if no errors have been detected. If no errors are detected, there is no reason to correct an error.

Claims 5-7 are dependent on claim 4 and therefore inherit the 35 U.S.C. 112, second paragraph issues of the parent claim. As such, these claims will not be given further consideration with respect to the art.

Claims 10-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites in part "...a trigger circuit that activates the third logic element when the shift register contains a bit sequence in which no erroneous bits have been detected." However, the third logic element as detailed in claim 8 (claim 10 is dependent on claim 8), is as follows "a third logic element that receives the output signal and corrects the actual (N+1)-th bit according to the output signal as the (N+1)-th bit propagates through the shift register." As such, the third element when activated will be correcting data without errors.

Claims 11 and 12 are dependent on claim 10 and therefore inherit the 35 U.S.C. 112, second paragraph issues of the parent claim. As such, these claims will not be given further consideration with respect to the art.

Claim 13 recites in part "...a trigger circuit that prevents the third logic element from correcting any bits until the shift register contains a bit sequence in which no error has been detected." Again, it is unclear why correction would be performed on bits with no errors.

Claim17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 17 recites in part "...suppressing any correction of the actual next bit until no error has been detected in a plurality of bits in the sequence." It is unclear why a correction would be necessary if no error has been detected in the bit sequence.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form 892.

The examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider

all of the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt 10/8/07
Cynthia Britt
Primary Examiner
Art Unit 2117